REMARKS

The Examiner rejected claims 1-2 and 15-16 under 35 U.S.C. 103 as being unpatentable over Jain (2003/0063517). Applicants believe this to be an error and that the Examiner meant to reject claims 1-2 and 15-16 under 35 U.S.C. 103 as being unpatentable over Jain (2003/0063517) in view of Thwaite(US 6,914,841).

The Examiner rejected claims 1-7 and 15-20 under 35 U.S.C. 112 (first paragraph).

Applicants respectfully traverse the §112 and §103 rejections with the following arguments.

35 USC § 112

The Examiner rejected claims 1-7 and 15-20 under 35 U.S.C. 112 (first paragraph), as "based on a disclosure which is not enabling. Paragraphs (0031) to (0032), after the activation of the word lines for write and read test patterns to and from the DRAM, the output patterns are compared to the inputted test patterns to determine which DRAM cells are connected to defective word lines or bit lines is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. *See In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Since claims 1 and 15 are* methods for testing a DDR DRAM. Therefore, they should include the essential step of comparing the output test patterns with the inputted test patterns to determine which DDR DRAM cells are connected to defective word lines or bit lines."

The Examiner appears to consider a step where "the output patterns are compared to the inputted test patterns" as being a necessary part of a claim combination as taught by the Applicants specification.

First, Applicants are confused as to how the Examiner can state both comparing is "**not** included in the claim(s)" and "**not** enabled by the disclosure" in support of a rejection based on *In re Mayhew*. Applicants point out a U.S.C. 112 (first paragraph) rejection based on *In re Mayhew* **requires** enablement in the disclosure of the invention. *In re Mayhew* states in part "We will sustain this rejection because we are convinced from the disclosure in the specification that appellant clearly regarded these steps as **essential** (emphasis added) steps in his inventive process. These steps are not recited in the claims." The Examiner has indicated that "comparing" is not enabled by the disclosure. If "comparing" is not enabled, then leaving out "comparing" cannot form the basis of a rejection requiring "enabling". Further, *In re Mayhew*

would require that the "comparing" be "essential in the inventive process", but Applicants do not disclose that the "comparing" is an essential step. Therefore, Applicants believe the Examiner rejection of claims 1-17 and 15-20 based on U.S.C. 112 (first paragraph) to be improper and request the rejection be withdrawn.

Second, Applicants maintain, that claims 1 and 15 have utility without the step of comparing "output" to the "inputted test patterns" as claims 1 and 15 describe a method of **obtaining** test data which is novel. Applicants point out that the actual comparing of data is often done well after the burn-in portion of testing is complete and could even be done by a party other than the party that did the actual burn-in part of the test.

Third, Applicants teach in paragraphs [0030/0031] that "Afterwards, the output patterns can be compared to the inputted test patterns to determine which DRAM cells are connected to defective wordlines or bitlines." Applicants maintain that this statement enables "comparing" as comparing of data is well known in the art, but does not teach the that the "comparing" is "essential" to the operation of the invention as required by *In re Mayhew*.

35 USC § 103 Rejections

As per claims 1, 2, 15 and 16, the Examiner states that "Jain discloses a method, comprising: a) Placing the memory banks in test mode; b) Issuing a bank activate command to select a word line for write of the memory) writing with auto-pre-charge, a test pattern to cells of the memory bank; d) repeating b) and c) until all world lines for write have been selected; e) issuing a bank activate command to select a word line for read of the memory bank; f) reading with auto-pre-charged, the stored test pattern from cells of the memory bank; and g) repeating c) and f) until all word lines for read have been selected."

As to claims 1 and 15, Applicants point out that Jain in FIG. 1 and paragraphs [0010] to [0015], [0025] and [0026] does not teach " (c) writing with auto-precharge" or (f) "reading with auto-precharge" as the Examiner asserts and as Applicants claims 1 and 15 require. Applicants point out that here is no mention of pre-charging in Jain et al.

Further, the Examiner asserts, "Jain does not disclose the memory is a DDR DRAM. However, Thwaite discloses that memory is a double data rate dynamic random access memory (DDR DRAM) (col. 1, lines 23-35). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention, to incorporate the DDR DRAM as taught by Thwaite into the invention of Jain to achieve a high speed operation during which two data transfers are made per clock cycle, one upon the rising edge of the clock and the other upon the falling edge."

Applicants point out that Thwaite is describing the normal operation of a DDR DRAM to "achieve a high speed operation" and there is no expectation that the method of Jain is applicable to a DDR DRAM or results in the benefit of "high speed operation" during testing which must be performed at low speed (because heating slows down the DDR DRAM).

Still, further, Applicants point that Jain is unable to test DDR DRAMs because Jain et al. does not take into account the write latency in DDR mode (data out on falling and rising clock edges) as taught in the background of the Applicants disclosure, so Jain can only test in SDR (data out on rising clock edge) mode.

As to claim 2, Applicants also point out that that Jain in FIG. 1 and paragraphs [0010] to [0015], [0025] and [0026] does not teach "each of steps (b), (c), (e) and (f) each take one clock cycle" as Applicants claims 2 and 16 require. Applicants point out that Jain is silent as to the timing of any of his signals, merely indicating that there is clock signal.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 2. 15 and 16 are not unpatentable over Jain in view of Thwaite and are condition for allowance. Since claims 3-7 depend from claim 1 and claims 17-20 depend from claim 15, Applicants respectfully maintain that claims 3-7 and 17-20 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0458.

Respectfully submitted,
FOR: Norris et al.

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